



**White Paper:  
Measuring the Value of Third Party Interconnects**

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According to Semico Research, the interconnect segment of the semiconductor intellectual property market will be \$77M in revenue for 2007, with a compound annual growth rate of 31%, or roughly double the rest of the SIP market. Interconnect revenue surpassed DSP revenue as a category in 2006. The explosive growth of the interconnect segment is a result of the continued acceleration of the complexity being driven into single chip systems and the need to architect complex data flow structures. Outsourcing the interconnect design has become increasingly more economical.

This paper discusses the economic benefits realized, when outsourcing complex SoC interconnect design and using Sonics SMART Interconnect solutions. The paper first uses a volume distribution for a cellular phone market segment as an example to show how small time to market advantages can have a dramatic impact on realized gross profits. Secondly, the paper uses an output production economic model to quantify the underlying productivity gains realized by outsourcing the internal interconnect design, which enables time to market improvements. Finally, the paper discusses the benefits of adopting an outsourced interconnect strategy as a basis for a platform-architecture that enables a family of products to realize compounding benefits.

### **Introduction: Its 2007..... SoC interconnect design is now center stage**

In 2005, when the first version of this white paper was released, the convergence of multimedia and communications was cited as a new trend changing the economics by which SoCs would be developed. In two short years, a lot has changed, all of which points to even stronger economic benefits.

#### Convergence Expands

Adding computing to the convergence definition, which previously only included multimedia and communications, increases interconnect design complexity in even further. Ultra Mobile PCs with WiFi/WiMAX, and mobile internet appliances, such as tablets and smartphones with wireless connectivity (running Linux and Windows CE), are growing in popularity. Companies developing these products are adopting SoC methodologies to address smaller market segments with shrinking life cycles.

#### Convergence Matures

The adoption of new communications and multimedia standards further increases data flow management complexity. Communications standards such as Bluetooth and WiMax are now complimenting cellular and WiFi standards in order to accommodate the transmission of higher quality content. As packet processing requirements increase, so does the need for more data to move more rapidly within and out of the SoC. Low latency arbitration schemes, when mixed

with multimedia and computing resources on the same chip, become even more difficult to develop as heterogeneous data traffic increases. Quality of Service is now a standard requirement to adequately address the balancing act arbitration schemes must maintain with sufficient performance to keep all IP cores satisfied.

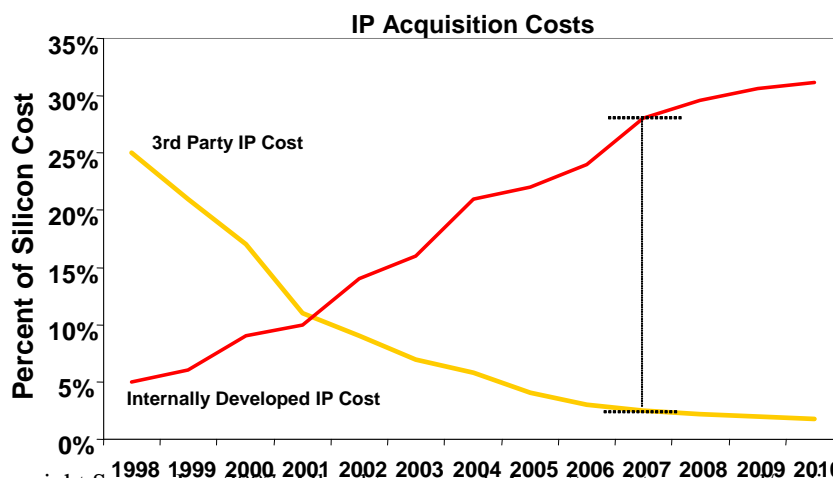
The explosion of high definition multimedia, prevalent today in mobile devices as well as home and business appliances is also causing significant processing upgrades and data flow management challenges. However, high definition is also now taxing the very fundamental interaction with external memory. The paradigm of one port access to DRAM is breaking down, as conventional DRAM technology cannot service the needs of the new content cost effectively. As DDR3 emerges, new methods of external memory access are required. This calls for closer coordination of the memory subsystem access, coming from a growing number of sources, with the arbitration schemes (QoS) in the interconnect, so that memory bandwidth can be optimized.

### OEMs changing their semiconductor supplier relationships

Single chip systems leave little hardware differentiation for OEMs. Emphasis on software and architecture is now the trend for OEM differentiation. As such, OEMs are designing more of the “front end” of the chips they use, in order to maintain their competitive advantage as portions of their software are expressed in silicon. This means OEMs and semiconductor suppliers are changing their relationship from the standard merchant supplier model to a new more interactive model by which OEMs can efficiently transfer their IP to semiconductor suppliers for SoC design completion and fabrication. Since many portions of the SoC are using commodity IP cores, such as embedded processors, DSPs, the differentiation emphasis is in data flow management. The interconnect represents a natural common ground between the OEM and their suppliers.

### Escalating Development Costs

Semico Research has recently updated its estimates about the cost of developing intellectual property. The following highlights the escalation of costs:



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Much of the rapidly rising development costs lie within the data flow management services required for Multicore SoCs, which is additional engineering over and above the wires that comprise a simple bus. The need for these services comes from the fact that SoCs today support multiple processing cores, a distributed computing methodology. Incorporating independent processing elements, such as DSPs and multimedia engines, create a need for system level management services (primarily for uniform IP core interconnectivity, QoS, power and security management). However, the host processor can only facilitate and not enforce these services on the chip. The interconnect then becomes the best source to manage these system functions.

Multicore SoCs also struggle with the traditional integration approach of coupling the computing and communications elements of the “system” into each of the IP cores themselves. These create tightly coupled systems that challenge system level verification and create long design cycles, as changing one component of the system cause the need to rebalance the entire system. In a complex SoC there are a lot of components to tune. The alternative today is to use interconnects that decouple the cores, by absorbing the communications within the interconnect, and separating the IP core through standard interface protocols. For distributed applications with heterogeneous processing elements, this is paramount to completing system level validation.

#### Risk management more prevalent than ever

Today, the minimum set of data flow services required for a Multicore SoC are: QoS, power management, security management and universal connectivity (the ability to accommodate several protocols so that IP cores in the library can connect seamlessly to the interconnect). This minimum set is sufficiently complex that above and beyond development costs for a SoC bus and the risks associated with internal design of these services can alone be a deciding factor to outsource the interconnect design. Acquiring these services as pre-designed and verified components increases the probability of the project hitting all its goals.

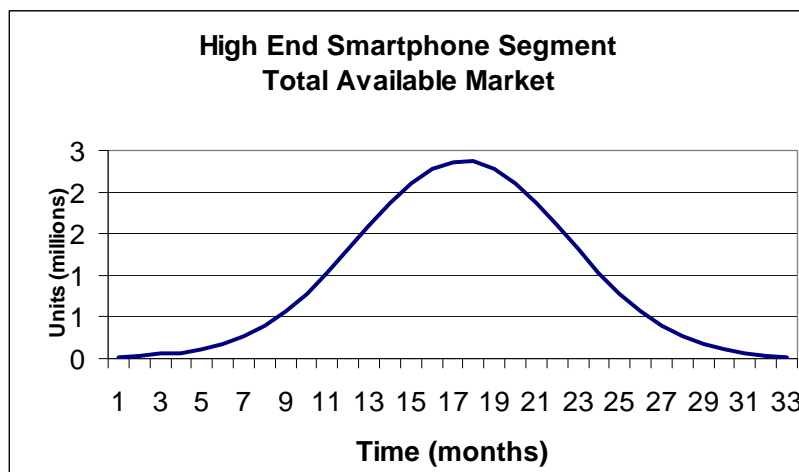
#### Complexity acceleration not slowing down

The common denominator for all the new trends is the SoC interconnect. With the cost of developing IP in house dramatically rising, and the returns for first-in growing, outsourcing the most critical portion of the SoC has become more economical from both a cost and a risk management perspective. As complexity continues to accelerate this too will remain the trend.

## Section 1: Quantifying the Impact of Outsourcing Interconnects

To highlight the economic shift favoring an outsourcing approach, this paper focuses on a segment of the smartphone cellular handset market. However, the economics discussed in this paper apply to many highly competitive, high volume markets. According to iSuppli, smartphone shipments in 2007 are projected to be 100 Million units. The rise in popularity of PC computing operating systems (Linux and Windows Mobile) within some smartphone models is creating a niche within the segment. This paper assumes the volume projections for such a niche will be roughly 10% of the overall market, or 10 million units for 2007. Since the paper uses a 32 month product life cycle, the total number of units available for the product are therefore assumed to be 30 million units.

The main feature requirements for the product to address this segment are connected to both 3G and WiMaX, with mobile video support and operating Linux or Windows Mobile. The distribution of the 30 million units Total Available Market (TAM) then is:



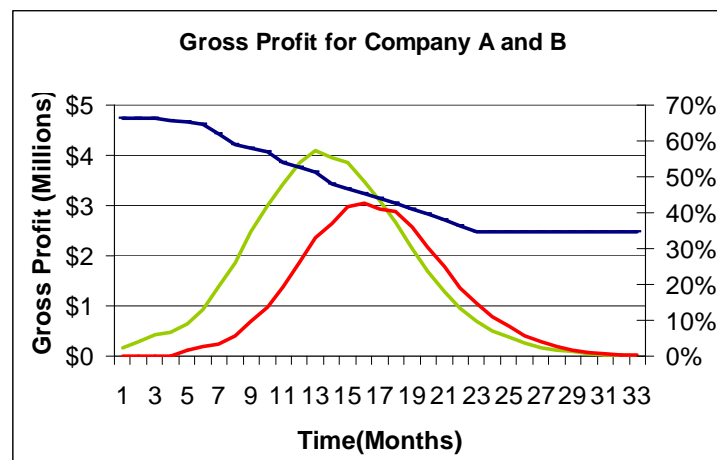
The complexity of smartphones means a Multicore SoC must be developed. Assuming that mature IP cores will be chosen as the processing elements, the dominant hardware development task will be interoperability of the processors and the bandwidth that can be achieved when accessing external memory.

The performance of the SoC interconnect will therefore have a high impact on the competitiveness of the SoC because of its high bearing on the utilization rates achieved for the processing elements. Variable data widths, complex arbitration schemes that can guarantee low latency to some processors and high bandwidth to others, security, error, and even power management, all effect the utilization of the processing elements on the chip, and must now be present to meet end user requirements. This creates the need for the data flow, in addition to the bus elements, in order to manage the heterogeneous multiprocessing.

As such, the paper will assume that the Multicore SoC interconnect is the most important design decision and will drive the overall SoC architecture. The paper will isolate the interconnect architecture as the one risk item (for the purpose of showing the economic shift) that can most effect the overall development cycle.

### Competitive Analysis

The research performed by Sonics modeled four competing companies in the segment (Companies A through D). Only the results of Company A and B are presented in detail. Suppose that Company A enters into the market with the first version of the product, and Company B enters the market 3 months later. What are the gross profits for Company A and Company B? Since this segment is highly elastic, it is very sensitive to time and price competition, overlaying an aggressive gross profit erosion curve (in blue below) over the distribution curves for Company A (in green) and Company B (in red) reveals the market dynamics:



Assuming that the market segment Average Selling Price (ASP) for the SoC starts at \$18 (\$11.30 cost @ 66% GPM) and drops to \$13.50 (\$10 cost @ 35% GPM) at month 32, Company A (in green) and Company B (in red) gross profits can then be estimated using the graphs above. The table below shows the spreadsheet calculations which highlight the impact on gross profit for the life of the product as a result of a 3 month delay in market entry by Company B.

	Revenue	Gross Profit	GPM
Company A	\$149M	\$48M	32%
Company B	\$112M	\$34M	31%

The results show that Company A enjoyed 33% more revenue and 41% more gross profits when compared to Company B. If the technical merits of both company's products are "normalized", that is both companies started their development cycles at the same time, using the same IP cores, software stacks, engineering talent, etc., what accounted for the difference in time to market?

Three months represents the difference in one spin on the design given the level of SoC complexity. One iteration of a the interconnect design and verification process can conservatively account for the 3 months.

Company A utilized a Sonics SMART Interconnect solution, which provides the necessary data flow services in addition to bus features to meet end requirements, and took advantage of SonicsStudio tool to accurately predict the data flow behaviors before and during the early phases of the chip design. The decision to outsource the interconnect lowered Company A's risk, "saving" 1 design spin when compared to Company B. This resulted in Company A capturing premium designs in the market that yielded the additional gross profit.

Company B, utilizing an in house design team, realized a similar interconnect solution but because it did not have the maturity and robust testing that Sonics SMART Interconnect solutions have, and did not have the same level of tools automation provided by SonicsStudio, Company B experienced 1 extra design spin and as a result lost out on premium sockets and realized lower profits.

**It is somewhat irrelevant that the in-house design team designed a similar interconnect solution as one that can be acquired from a third party. What is important was that Company A reduced a major risk item in the SoC development process by deciding to outsource the interconnect design, beat Company B to market and boosted its revenue and profitability significantly as a result.**

It is also worth mentioning that a second advantage of outsourcing the interconnect is the accommodation of market requirement changes late in the design cycle. Since Company A chose a flexible solution, making changes to any of the cores, or the interconnect itself, are virtually independent events that can be isolated to minimize re-engineering, a benefit of modularity and the decoupled methodology. These changes are only incremental to the overall development process and top level verification is still reached in a much faster time.

**One spin in highly elastic markets can have a huge impact on success.**

## Risk Factor Analysis

The method used to assess risk for this example comes from the Risk Factor Analysis paper written by John Kindinger and John Darby of the Los Alamos National Laboratory. In this analysis four risk factors are identified:

1. Technology risk – The requirement for new technology to complete the project
2. Schedule risk – The ability to accurately plan and scope tasks for the project
3. Cost risk – The ability for the project to achieve the planned life cycle costs. This includes development of the technology in-house and the maintenance of the technology over the life expectancy of the product (assuming derivatives)
4. Funding risk – Assess the risk of available funding for the project when needed. This focuses on EDA expenditures, as well as any additional labor required to complete the project.

Each of the risk areas will be assessed based on comparing in-house versus outsourcing using a Sonics SMART Interconnect solution.

### Assessing Technology Risks

This project requires all of the convergence elements as modes of operation for the SoC:

1. IP core selection
  - a. In-house - Assuming adequate commodity libraries are available and processor upgrades or the addition of DSPs or multimedia engines are also readily available, this was graded as low risk
  - b. Outsourced – Sonics supports the seamless connection of any OCP or AMBA core selectable on a port by port basis. Sonics has also connected to several customer core interfaces with trivial complexity in the bridging. As such, the outsourcing approach would maintain the same level of connectivity ease and this task was also rated low risk.
2. IP core connectivity and interoperability -
  - a. In-house - Given that there are combinations of low latency, high performance and random access requirements, the arbitration scheme required to accommodate all these needs is very complex. It is assumed that such a complex scheme has not been developed previously. The lack of available technology makes this a high risk task.
  - b. Outsourced – Sonics supports advanced arbitration with adequate QoS to accommodate this project. Having the pre-verified

technology available at the start of the project reduces this task to low risk.

3. Development of data flow services -
  - a. In-house- The ability to engineer a QoS scheme as well as system wide power and security management are complex tasks and the lack of technology available at the start of the project makes this a high risk task.
  - b. Outsource – Conversely, the existence of pre-verified technology available by adopting a Sonics SMART Interconnect solution, which supports low power system management, security management (including firewalls) and has a comprehensive QoS scheme as part of this standard offerings, reduces this task to low risk.
4. External memory design –
  - a. In-house - Multiple sources accessing external memory make memory scheduling a requirement. Additionally, assembling disparate components (memory scheduler, DRAM controller, and PHY) to achieve high bandwidth using DDR2 raises the level of risk for this task significantly. Often teams must iterate on the subsystem development to achieve such high efficiency. This is a high risk task.
  - b. Outsource – Sonics offers two flavors of memory scheduler. MemMax enables efficient memory scheduling and can attach to any DRAM controller. MemMaxRD has been optimized for Synopsys Designware DRAM controller such that high bandwidth can be achieved using Sonics' verified out-of-the box memory subsystem solution. Having a high bandwidth solution available at the start of the project reduces risk to low.
5. System validation –
  - a. In house - Unit level validation is still a task well suited for EDA tools. However, the lack of adequate tools for system level verification translates into very long debugging sessions at or near top level integration. The lack of technology suited to mitigate this late in the design cycle system debugging makes this task high.
  - b. Outsource – SonicsStudio tool can be used to configure and model (using statistical modeling) the behavior of data flows. The ability to model data flows during the architecture development enables engineering teams to shift verification risks by avoiding lengthy debug sessions and eliminate uncertainty of the design and as such this task is reduced to low risk.

### Analysis of Schedule Risks

It is assumed that all companies possess adequate expertise to develop the interconnect architecture for the project, and that the team of experts required to execute this will be assigned to the project. On this basis, the following was the analysis of schedule risk:

1. Project scoping
  - a. In-house -Given that interconnect architecture experts are available, it is assumed their ability to comprehend and adequately scope the project results in an accurate schedule. Because of the complexity their will be some level of uncertainty. As such, this was rated as medium risk.
  - b. Outsource – While much of the benefit of having an outsourced interconnect solution is comprehended in the technology risk assessment section, eliminating many complex tasks reduces the uncertainty in the scheduling of the project. Therefore, this was reduced to low risk.
2. Research and analysis –
  - a. In-house - This factor relates to the amount of preparatory work that those individuals associated with the early stage of the project undertook to arrive at their scheduling estimates. No EDA tools exist today that allow pre-chip statistical development of data flow paths. Since it is assumed that the combination of elements to be used in the project are new from a system integration perspective, this is rated a high risk task.
  - b. Outsource –SonicsStudio enables statistical modeling of the data flows to achieve high performance and predictability before the chip development. This tool also allows for what if analysis, which contributes significantly to any architecture research, and as such reduces this risk to low.
3. Labor availability
  - a. In house - Resourcing the project for a significant period of time, and at an opportunity cost of engineering other projects, assuming reasonable discipline and no major impact to schedule based on the lack of availability of key expertise, keeps this task at medium risk.
  - b. Outsource – Since this option eliminates a reasonable amount of significant technology risks from the project, the ability to mix staff in order to limit high skilled individuals without jeopardizing the project reduces the risk factor to low.

### Analysis of Cost Risks

Assuming an SoC hardware development cost is \$40M, software development is assumed to be another \$40, with half of that cost incurred by the OEM. The project costs then is \$60M.

1. Initial cost risks
  - a. In-house -Based on the estimates above, and assuming that adequate margins can be reached relative to resultant die size (yield) and package and test costs, this was rated as a low risk.

- b. Outsource – It has been shown in this paper that the relative acquisition cost of an outsourced interconnect solution does not add significantly to the project costs. Therefore, this task is also rated low
2. Maintenance costs:
    - a. In-house design –The ability to maintain the highly skilled team after the project completion is unlikely given other projects in the company would need similar expertise. Therefore, the architecture maintenance would be passed on to a new team, or a subset of the original team. This poses significant risk given the high level of complexity and as such this task was rated high risk.
    - b. Out source – Shifting many of the complex engineering tasks to an outside vendor significantly eliminates the risk associated with maintenance. Therefore this is left also as a medium task.
  3. Opportunity cost
    - a. In-house - The cost of maintaining the highly skilled team to complete the interconnect architecture given a long design cycle was assumed to be moderate in the schedule risk assessment. To remain consistent, this task was also rated as medium risk.
    - b. Outsource – Off loading the team from significant engineering tasks enables them to work on differentiable aspects of the project, or to start derivative projects earlier, either of which improves the opportunity cost and reduces the risks to low.

### Assessing Funding Costs

Using costs from the previous section the funding risks were assessed as follows:

1. Base line project funding
  - a. In-house - It is assumed that the company can afford the \$60M for this project, while not severely hampering other business unit projects. The baseline funding risk then is assumed to be medium.
  - b. Outsource - The cost of acquiring the technology does not materially shift the funding costs and as such this is also rated medium.
2. Ancillary funding costs
  - a. In-house - In the event that the project needs more engineers or more tools to complete the project, it is also assumed that all companies have adequate funding to supply the engineering team with the additional needs, and that the high priority nature of this project would justify the expenditures. This task was then assumed to be medium risk.

- b. Outsource – The availability of SystemC models and the SonicsStudio tool greatly reduce the need for ancillary funds to develop representations of the same. Therefore, this is reduced to low risk.
3. Return on Investment –
- a. In-house - First time working silicon must be achieved and the resulting product must also return high profits for the company. Therefore, the risk of project overruns in cost and time have a significant weight in the ability for the company to enter the market and secure premium sockets at high gross margin. Late entry means severe gross margin penalties. Extreme market elasticity makes this ROI achievement high risk.
- b. Outsource – Eliminating significant technology and schedule risks as a result of adopting an outsource solution improves the chances of first time working silicon. The flexibility of the solution also allows for late definition changes and for better predictability forward looking into the derivatives planned for after the initial project. These directly impact the ROI risks and as such this task is reduced to medium.

### Summarizing the Risk Analysis

The following table summarizes the findings of the risk analysis. A numerical score was given to each rating, low=1 point, medium=2 points, high= 3 points. A second analysis which offers heavier weighting into the most critical elements of the project is also offered. Numerical risk scores in these were doubled.

Non weighted	In House	Outsource	Weighted	In House	Outsource
<b>Technology Risks</b>	<b>13</b>	<b>5</b>	<b>Technology Risks</b>	<b>22</b>	<b>5</b>
IP core selection	1	1	IP core selection	1	1
IP core connectivity	3	1	IP core connectivity	3	1
Data flow Services	3	1	Data flow Services	3x2=6	1
External memory	3	1	External memory	3x2=6	1
System validation	3	1	System validation	3x2=6	1
<b>Schedule Risks</b>	<b>7</b>	<b>3</b>	<b>Schedule Risks</b>	<b>10</b>	<b>3</b>
Scoping	2	1	Scoping	2	1
Research	3	1	Research	3x2=6	1
Labor availability	2	1	Labor availability	2	1
<b>Cost Risks</b>	<b>6</b>	<b>3</b>	<b>Cost Risks</b>	<b>6</b>	<b>3</b>
Initial costs	1	1	Initial costs	1	1
Maintenance costs	3	2	Maintenance costs	3	2
Opportunity costs	2	1	Opportunity costs	2	1
<b>Funding Risks</b>	<b>7</b>	<b>5</b>	<b>Funding Risks</b>	<b>7</b>	<b>5</b>
Base line	2	2	Base line	2	2
Ancillary	2	1	Ancillary	2	1
Return on invest.	3	2	Return on invest.	3	2
<b>Total</b>	<b>33</b>	<b>16</b>	<b>Total</b>	<b>45</b>	<b>16</b>

The analysis indicates clearly that outsourcing the interconnect reduces project risks by over 50% in both the weighted and non-weighted cases. A significant reduction in technology risks account for a large portion of the savings, but the ripple effect through the schedule, cost and funding risks are also noticeable. This supports the basic principle that efficiency gains should be realized as a result of technology acquisitions (discussed in detail in the next section).

Additionally, the assumptions made were a conservative view of the risk assessments. The variability of these assumptions can be high and could have a significant impact on the analysis. For example, it was assumed that scoping and scheduling for the project was accurately portrayed by the engineering team and held throughout the program. Any project challenges not accounted for, such as architecture rework as a result of incorrect assumptions made at the beginning of the project, or delays in IP acquisition, would certainly have an effect on the risks and the outcome of the study. Since this is more likely to happen when engineering in house solutions (a lot more complex tasks to engineer) the sensitivity to this effect is high but relatively low for outsourcing (because there are far less complex tasks as a result of acquiring pre-verified technology).

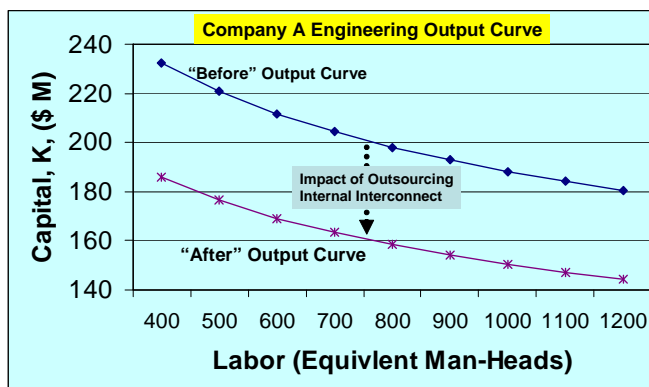
## Section 2: Why Outsourcing Interconnect Improves Productivity

Why does outsourcing the interconnect result in faster time to market? The answer lies in looking at the impact of introducing new interconnect technology innovation in light of a capital and labor mix for a company that defines the pace of its output production versus expending labor to create a similar solution.

In the following example, the output productivity levels were held constant and capital and labor mixes varied to show how the outsourcing decision of Company A enables them to realize a time to market advantage over Company B.

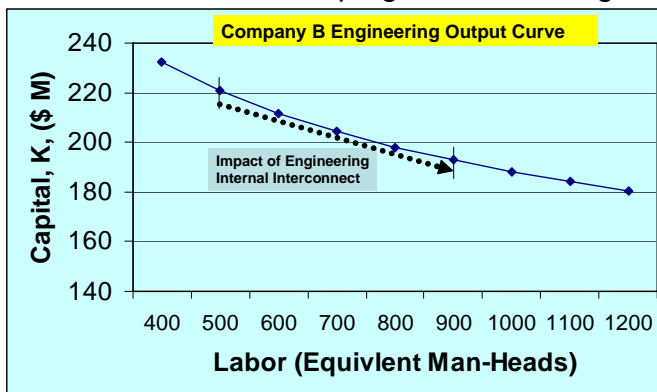
Consider the following output curve of the SoC development team for Company A. The “before” curve represents the estimated capital and labor costs for Company A to develop their share of the SoCs over a 32 month period, based on its tools chain (capital) and its team size and expertise (labor). The net effect of purchasing a

Sonics SMART Interconnect solution is a technology input that makes the tool chain and labor more efficient. As such, it serves to permanently shift the entire productivity of Company A’s SoC development team to the “after” curve. Company A can now produce the same amount of output more efficiently.



This has significant ramifications for Company A, because using a platform strategy, Company A can now deliver more products with the same labor force faster than before. Section 3 will quantify the compound benefits of this shift.

Now consider Company's B decision to invest in developing and sustaining the interconnect. The decision has a different impact on output because there is labor burden to engineering an equivalent solution in lieu of a technology input. Therefore Company B's "make" decision serves only to move their output from point A to B on the same output curve, but does not shift the curve.



The added labor investment made by Company B is not justified, because Company A's "buy" decision actually impacted a greater change in output productivity. Since Company A and B started with the same output curve, Company A has a sustainable competitive advantage.

Given that "buy" in principle is a better decision over "make" then, the next item is to quantify the cost of adopting the two approaches to ensure purchasing the interconnect does not outweigh its benefit. The table below represents Sonics' estimates of the comparative costs of the two approaches:

	Acquisition Cost	Development Time (Man Months)	Labor Costs (\$20K per MM)	Maintenance Labor	Maintenance Costs (\$20K per MM)	Total Cost
<b>Company A</b>	\$500K	2	\$40K	15% of AC	\$75K	\$615K
<b>Company B</b>	0	30	\$600K	4 manmonth	\$80K	\$680K

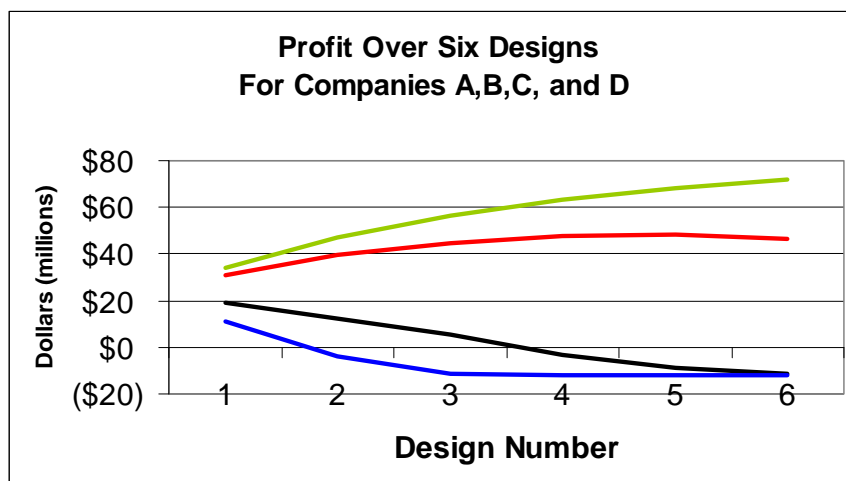
The total costs are relatively the same, preserving the economic benefit realized by Company A.

### Section 3: The Compound Benefits of an Outsourced Interconnect Strategy

This paper has focused on a single product design. In this section the results of a platform strategy are quantified, which is a series of products derived from the base design in order to show the benefits of an outsourced interconnect compound over time.

Looking back at Company A, their decision to outsource enabled them to secure a better market position. This has three advantages. First are more profits which can be invested to improve its business even further. Second is increased market share relative to its competitors; and third is increased engineering output with lower design risk which enables Company A to start and complete more projects even faster.

Company A will gain even more volume, more profit, more market share, and also start new projects even earlier as time passes. Company A realizes compounding profits then that can be shown below (over 6 designs over 133 months in this example):



While this paper focused on Company A and B, the research conducted for this paper was conducted over four companies each entering the market in 3 month intervals and all except Company A maintaining in-house internal interconnect solutions.

With compounding profits quantified, it is easy to see increasing ROI for Company A even though it continues to increase its investment in purchasing interconnects over time. In the above analysis, Company A achieves \$82M more in profit over the 6 designs when compared to Company B, \$327M more than Company C and \$380M more than Company D.

The dramatic drop off in profitability that Company C and D experience is attributed to their late entry into a market whereby most of the premium designs

are already consumed by Company A and B. Correspondingly, severe market gross margin erosion is putting enormous pressure on Company C and D operations to hold costs down, at a time when two of their competitors thrive. The additional two data points are provided to highlight that relative small additional delays (6 month delay for Company C relative to Company A), have dramatic effects on success in highly competitive markets.

## **Final Thoughts**

Basic economic principles were used to show that given that high complexity interconnect solutions are required to meet the needs of SoCs in the convergence era, it is more economical to buy them rather than make them. The assumptions made in this paper are conservative given that convergence is accelerating, forcing even more challenging requirements over time that make complexity grow exponentially.

This paper did not discuss in detail the effects of competition beyond the first two companies, other than anecdotally introducing Company C and Company D to show how rapidly the profit potential of a highly competitive market can erode.

Additionally, only 1 product development scenario was discussed in the paper. However, the conclusions made are consistent with the semiconductor industry trend showing that utilizing third party IP has become more economical than internally designing and maintaining an equivalent.

This paper represents the state of the semiconductor industry today. Winning and losing in competitive markets are often established in the early months of a new segment's emergence. These markets often commoditize rapidly. Since the business of engineering complex SoCs is much more complex than it was in the past, the decisions that determine a company's potential competitive advantage (and thus its ability to win) must now be anchored in sound economic decisions as well as having clear technical merits.

By "normalizing" the technical merits between the solutions (assuming that both companies in the example eventually realized similar products), this paper highlights the vital importance of the economic components, including risk analysis, in the decision making process. Since multicore SoC interconnect is the most critical component of the SoC design, the risks related to interconnect design and verification now determine the overall project's success or failure.

For complex SoCs, it is no longer economical to maintain in house internal interconnect architectures because they now require an additional level of data flow service that must be engineered and maintained in addition to the bus features in order to meet end requirements. Sonics SMART Interconnect solutions represent a dramatically lower risk alternative that can mean the difference between winning and losing.