

## Product Brief

### On-chip Network Configuration

- Powerful tool to simplify the configuration and assembly for SoC connectivity
- Allows Sonics and 3rd party IP to be pulled into a variety of popular integration environments
- IP wizards allow easy, out-of-the-box configuration of complex SoC configurations

### Interoperable Open Standards

- Supports open standards including: Eclipse, IP-XACT, etc.
- Open platform scales with user needs and easily integrates into existing design flows

### Modular and Scalable

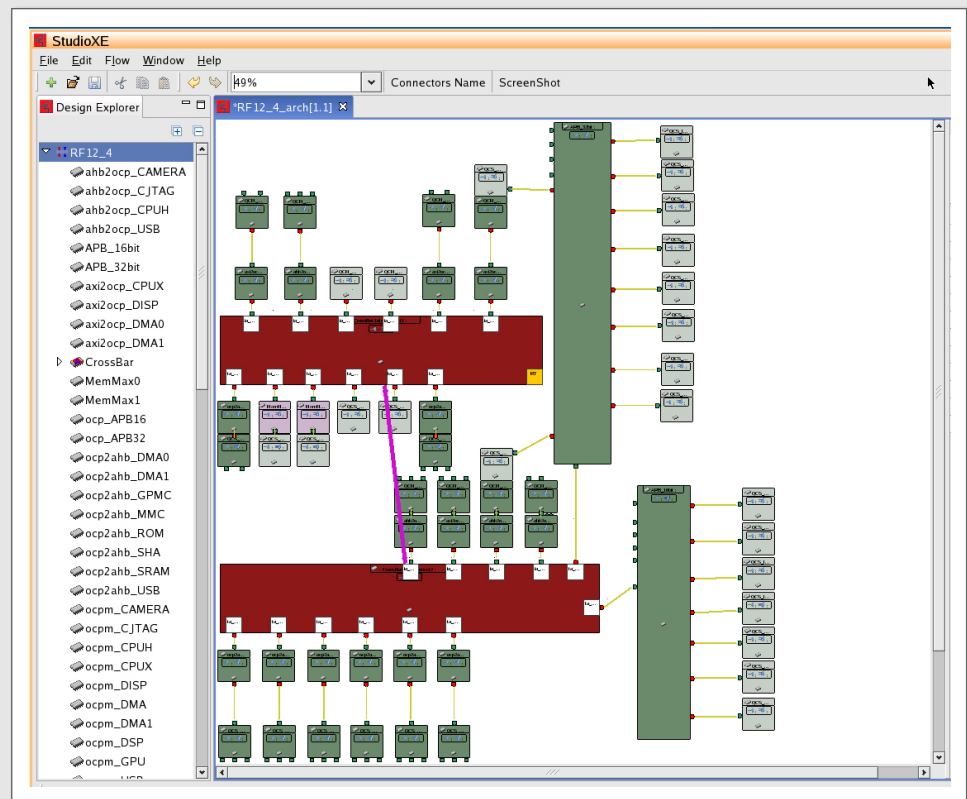
- Modular framework allows users to plug-in Sonics proprietary as well as 3rd party tools
- Performance Analysis, HW Performance Monitor, Interface Protocol, Register Management, etc.

### System Level Design Enabler

- Complete system design solution = IP + SW drivers + models + tool environment

Sonics' StudioXE is a next-generation, modular, system-level design tool which enables the rapid integration and configuration of Sonics on-chip network IP for complex SoCs. StudioXE contains a variety of modules and components which allow designers to easily incorporate Sonics innovative on-chip communications IP into their SoC design flows. By compartmentalizing StudioXE's functionality, Sonics has created a tool that enables small, fabless semiconductor companies as well as top tier semiconductor manufacturers to access and assimilate Sonics silicon proven technology across their SoC portfolio.

In addition to the StudioXE framework, Sonics has created open wrappers for its entire line of semiconductor IP, allowing these components to be pulled into almost any design environment. Because StudioXE is based on the open Eclipse framework and uses the industry standard IP-XACT metadata format, users can easily pull Sonics IP into their specific design flow without having to worry about compatibility issues or moving into a different tool to be able to configure the IP. If you do not have your own design cockpit, StudioXE also includes its own full design environment allowing easy configuration of Sonics and other 3rd party IP.

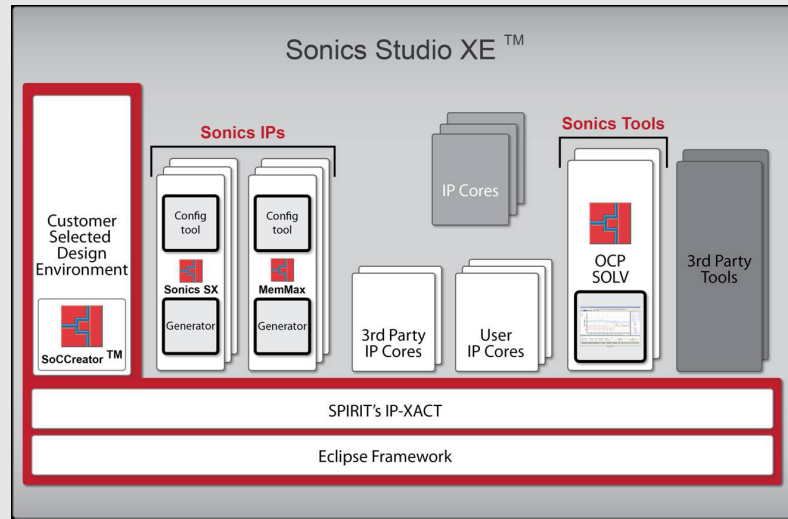


## StudioXE Features and Components

### Design Environment

Depending on flow and methodology requirements, users will have different needs with respect to the design environment they choose for the development of their SoCs. Some designers may have their own custom environment, either customized from a third party tool, or developed internally from the ground up. For these users, Sonics IP can be instantiated directly in their custom environment provided it supports the IP-XACT metadata format. Other users may be using a design environment provided by a third party such as Cadence, Atrienta, or Magillem. In these cases, Sonics has already worked with these vendors to ensure that Sonics IP can be opened and configured from within these tools. This provides a seamless system design environment whereby all pieces of the IP the customer chooses to work with can be implemented from within a single tool. For designers interested in a complete SoC design solution, Sonics provides the Sonics Design Environment as part of StudioXE. The Sonics Design Environment is a state-of-the-art tool enabling complete configuration of not only Sonics IP, but also the other master and slave cores which comprise the totality of the system. The Sonics Design Environment is made up of two parts: the System Assembly tool and the IP Packager.

# Sonics StudioXE



## System Assembly Tool

The Sonics System Assembly Tool (SAT) is a comprehensive solution for rapid SoC assembly and configuration. The SAT provides users with a graphical interface by which various cores can be connected with Sonics on-chip networks and memory products. These products can be customized to the unique needs of each specific implementation, allowing designers to tweak almost every aspect of the Sonics IP. The Sonics SAT offers a number of improvements and enhancements to those familiar with SonicsStudio SOCCreator product:

- User interface and usability improvements
  - Fast design load time
    - No matter the design size, loading time is fast and efficient
  - Smart placement of blocks
    - Automatic instantiation of blocks (like isolation cells for power management or bridge/abstraction adapters for regular connections) are placed “smartly” within the design space: spaced accordingly and as close as possible to the ports they are connected to
  - Smart signal and channel routing
    - Signals are easily routed around blocks and cores and routing can be user controlled.
- Global Connectivity
  - Connect ports across hierarchy levels without manually navigating the entire design (especially useful for clock and reset connectivity)

## IP Packager

The IP packager allows users to package their cores in an IP-XACT package enabling them to share, distribute and reuse their cores within and outside of the Sonics Design Environment. Sub-systems can also be packaged and distributed in much the same way. The IP-XACT standard allows designers to define visible levels of hierarchy within the subsystem itself. This packager facilitates designers' desire to import and export cores easily, allowing for interoperability and for

ease of sharing between tools and chip generations.

The IP Packager enables the creation of an IP portfolio that can easily be shared across large organizations and between different design tools.

## Sonics IP modules

With the introduction of StudioXE, Sonics is also refreshing the way its IP is packaged, making it more open and portable across environments and software platforms. This packaging is based on IP-XACT which allows the IP to quickly and easily be pulled into and configured in a variety of popular design environments. The IP modules will include the configuration tool of the IP as well as its IP generator. This combination allows the IP to be portable and self-contained, plugging into any environment and working without needing any separate software infrastructure around it.

## Configuration Tool

The IP Configuration Tool allows the customer to use a variety of standard input parameters to tweak the Sonics IP to suit their specific project and need. Architects have as much (or as little) input over the configuration of the IP as they desire. Built-in performance feedback monitors give real time updates to configuration changes, noting how design tweaks affect things like: minimum latency, max throughput, max frequency, gate count, power, and more. This real-time feedback is invaluable as designers aim to squeeze every last bit of performance they can out of their designs.

## IP Generator

The IP Generator within each Sonics IP module allows for the generation of a wide variety of outputs based on user needs and license. The modular structure of the output parameters ensures that users need only pay for the output format which they require. This enables per user licensing options without limiting the variety of possible output formats. Available output formats include: RTL, Verification, SystemC, Performance Analysis Instrumentation, IP documentation, software drivers, and IP Parameter description.