

## Product Brief

- Rapid configuration, modeling, and timing closure for SoC architectures based on SMART Interconnect solutions
- Reduces SoC development costs
- Enables collaborative development between SOC architects, RTL Designers, and Software Developers
- Reduces system verification risks
- Provides modeling and test benches that enable system verification during the SoC architectural phase
- Supports industry standard simulation, verification, and synthesis tools
- SonicsStudio operates on Linux Red Hat Enterprise Workstation 3.0 and 4.0, SUSE Linux version 9, and Solaris 5.8 and 5.9

The SonicsStudio development environment accelerates every stage of System-On-Chip (SoC) design. From architectural exploration to synthesis, SonicsStudio provides an array of graphical and command line tools that provide SoC architects and designers a single environment within which the entire SoC can be assembled, configured, simulated, and final netlist generated.

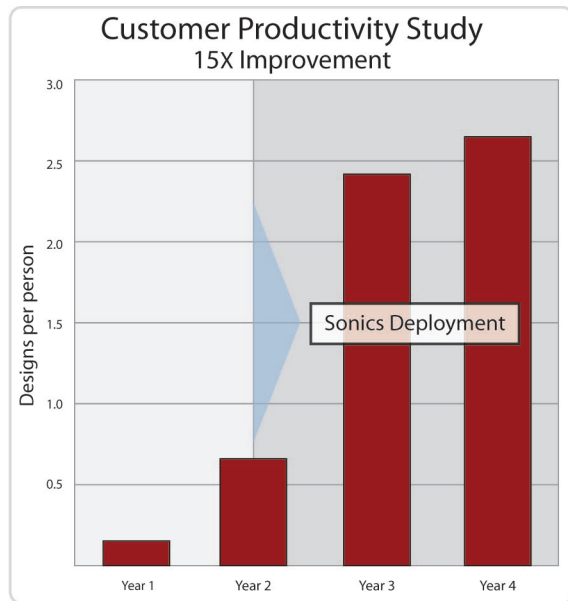
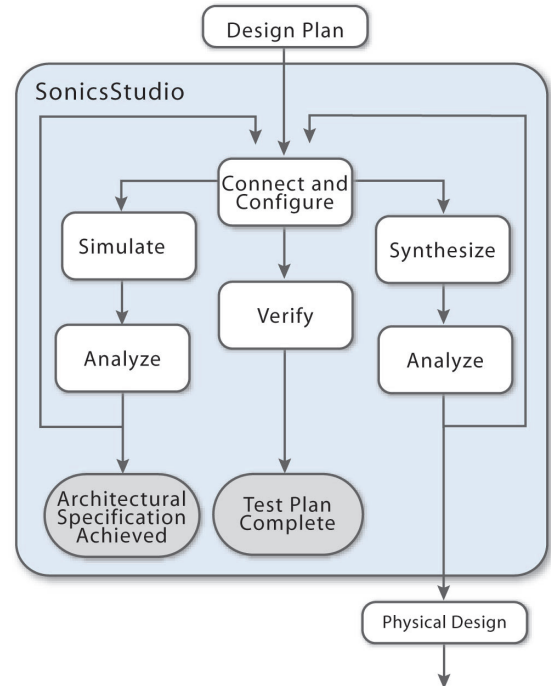


Using SMART Interconnect<sup>™</sup> solutions from Sonics, designers can instantiate all of the SoC cores, configure the interconnect, create functional models for those IP cores not yet available, place monitors, stimulate the SoC components and analyze the resultant performance of the interconnect using either SystemC or RTL. Within minutes, changes can be made to the interconnect, or the whole SoC can be re-architected for subsequent analysis. In this way, SoC architects can rapidly decide on the optimal SoC architecture that meets design and customer requirements.

SonicsStudio streamlines physical integration and validation for SoCs that incorporate Sonics SMART Interconnect solutions. Seamlessly integrated with tools for simulation, design, synthesis, and timing analysis. SonicsStudio eliminates time consuming design work by automating synthesis script and constraint creation, timing analysis input preparation, and design-for-test management.

## Features

- Assemble and configure complex SoC designs with an easy-to-use graphical user interface.
- Provides intelligent configuration dialogs for each module in the design, allowing early fine tuning.
- Offers behavioral models with customized traffic generation for architectural exploration using both SystemC and RTL level simulations.
- Facilitates performance analysis by utilizing built-in monitors and performance observation points that collect simulation and performance data.
- Supports configuration, verification, and analysis of OCP and AMBA (AXI, AHB, APB) protocols.



Year	Designs	Designers	Technology
1	2	14	Internal Design Team
2	12	18	Transition
3	17	7	Sonics-based Designs
4	24	9	

- Supplies automated testbench generation, simulation testing, and error checking for Sonics SMART Interconnect solutions.
- Allows plug-in of industry-standard simulators from Mentor Graphics, Cadence, and Synopsys.
- Supports the Open SystemC Initiative reference simulator and integrates with third party Electronic System-Level design tools.
- Offers a Sonics compiler that generates either Verilog RTL or SystemC designs at the push of a button.
- Enables automatic and consistent synthesis runs by simply specifying high-level technology and frequency requirements.
- Interchanges data with SPIRIT consortium compatible tools.