

Product Brief

The SonicsSX On-chip Network combines advanced fabric features and comprehensive data flow services architected for high performance multicore and multisubsystem SoCs

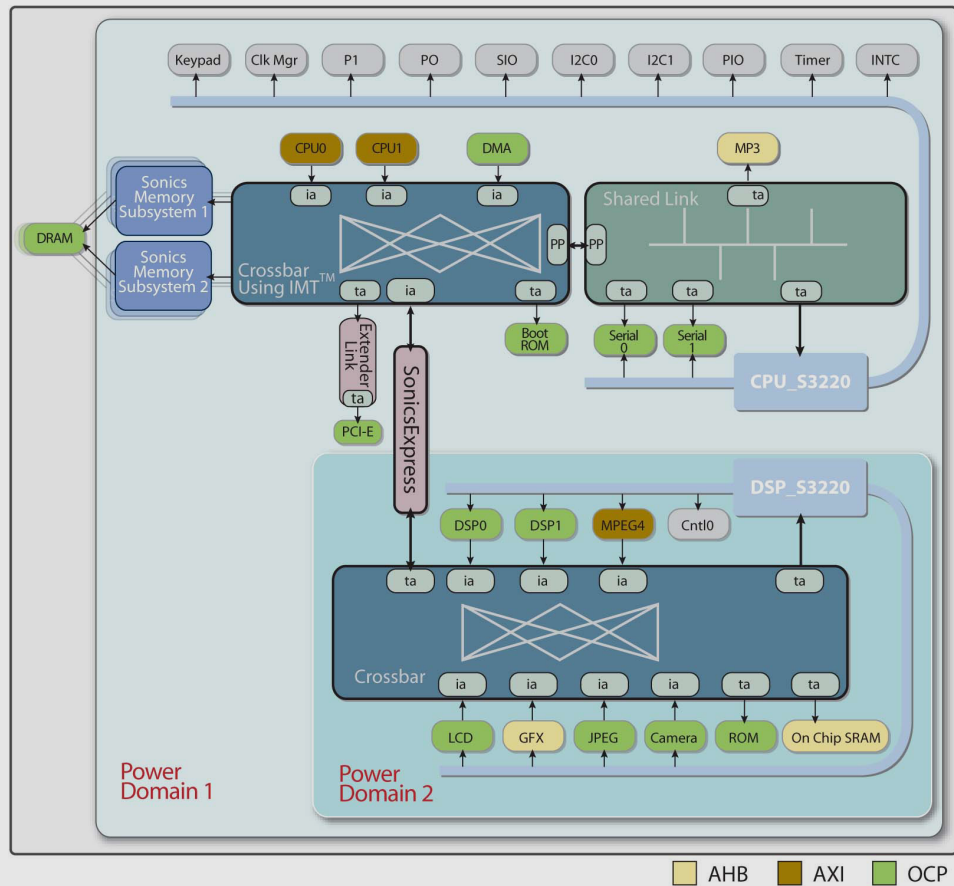
Support for high performance video data throughput:

- OCP 2.2 2D Block Read/Write, 256 bit data widths, and comprehensive quality-of-service to support over 10 GBytes/sec per socket, and 320 GBytes/sec per instance as a local subsystem interconnect solution
- Advanced fabric features and data flow services
- Contains IMT for Multichannel memory management support of DDR2 and DDR3

Advanced Fabric Based on Technology Innovations

- Low Latency Network on a Chip ensures high performance
- Multithreaded non-blocking flow control for maximizing system performance (BW/latency/power) in light of limited access rates to external memory resources
- Practical GALS extends asynchronous capabilities to include IP core or subsystem voltage and clock domain isolation
- Run time software programmability enables real time system control

The SonicsSX[®] On-chip Network contains a high performance, advanced fabric and a comprehensive set of data flow services for the development of complex, multicore and multi-subsystem SoCs. By utilizing state-of-the-art physical structure design and advanced protocol management, SonicsSX can act as a local subsystem or global interconnect solution. For video data throughput acceleration, SonicsSX supports higher operating frequencies via an NoC fabric, data widths up to 256 bits and 2D transfers. SonicsSX achieve up to 16 Gigabytes per second throughput per port. As a global interconnect solution, SonicsSX also supports advanced leading edge, fine-grained power management, quality-of-service, access security, hardware monitoring/debug ports, and error handling features that facilitate higher design predictability and decrease chip development time. In addition, SonicsSX allows SoC developers to easily transition from single channel to multiple channel external DRAM memory architectures seamlessly and transparently to software and hardwired initiators.



This example SoC utilizes the flexible topology and multi-channel features of SonicsSX, while employing Sonics3220[™] to partition slow speed peripherals, the Sonics MemMax[®] memory subsystem solutions to achieve high performance DRAM memory management and SonicsExpress[™] to support clock and voltage domain isolation. This example utilizes IMT multichannel memory management capabilities for two channels of external DRAM which enables throughputs up to 16 Gbytes per sec per port to be achieved while implementing quality of service guarantees across the entire SoC.

SonicsSX On-chip Network

Features

SonicsSX is a member of the Sonics family of On-chip Network products. Complementary products include MemMax™, an advanced memory subsystem solution, and Sonics3220™, a peripheral interconnect that off-loads slow transfers from the system interconnect. Key features include:

- NoC communications for high operating frequencies
- Practical GALs support allows voltage and clock domain isolation configurable on a per port basis
- IMT multichannel memory management for high memory bandwidth and DDR3 burst width conversion
- A total of 64 sockets can exist on each SonicsSX instance
- Configurable to include full or partial crossbars and/or shared links
- A highly flexible structure to accommodate latency sensitive portions of the system
- User-specified connection map, address map, and command map
- Permits internally shared paths
- Natively supports OCP 2.x sockets, and provides interfaces to OCP 1.0 sockets, AXI 3.0, and AMBA AHB-lite 2.0 sockets
- Implements dynamic endianness aware width conversions
- Configurable address widths up to 64 bits
- Target core address decoding down to a granularity of 1 KB
- Configurable protected regions within address space
- Supports BLCK burst sequences on OCP2 sockets
- Configurable data path widths (sockets and internal) 16, 32, 64, 128, or 256 bits; four to one range of widths allowed within any instance
- Peak bandwidth limited only by target limitations
- Accommodates synchronous and synchronous-divide clock rates for each socket
- Flexible internal pipelining makes frequency independent of span
- Supports 0 cycle minimum latency paths
- Supports differential quality of service (low latency, allocated bandwidth, best efforts)
- Supports sideband signaling for interrupts, errors, and power controls
- Scalable frequency, trading off interconnect span against latency by adjusting the depth of the interconnect pipelines
- Minimized active power consumption using streamlined internal protocols and a physically-aware structure
- Power management interface coordinates voltage or clock removal
- Implements fine and coarse grained clock gating for low idle and active power
- Monitors for software error conditions (unsupported commands, addressing errors) and protection violations
- Monitors for failing cores (timeouts)
- Performs error logging and recovery support
- Optional debug ports to probe operation of internal paths
- Quality-of-service management assuring predictable performance for real-time data flows
- Dynamically configured access protection (firewall) for cores or memory regions against access by specific initiating cores or processes
- Separate request and response networks that adapt easily to target agents with long or unpredictable latency (such as DRAM systems)