

## Product Brief

### Improves SoC Performance

- Isolate slow speed I/O from high speed SoC interconnects and consolidate I/O traffic to and from the SoC interconnect
- Deterministic response supports real time applications
- Built in security feature provides hardware firewall for system and media integrity

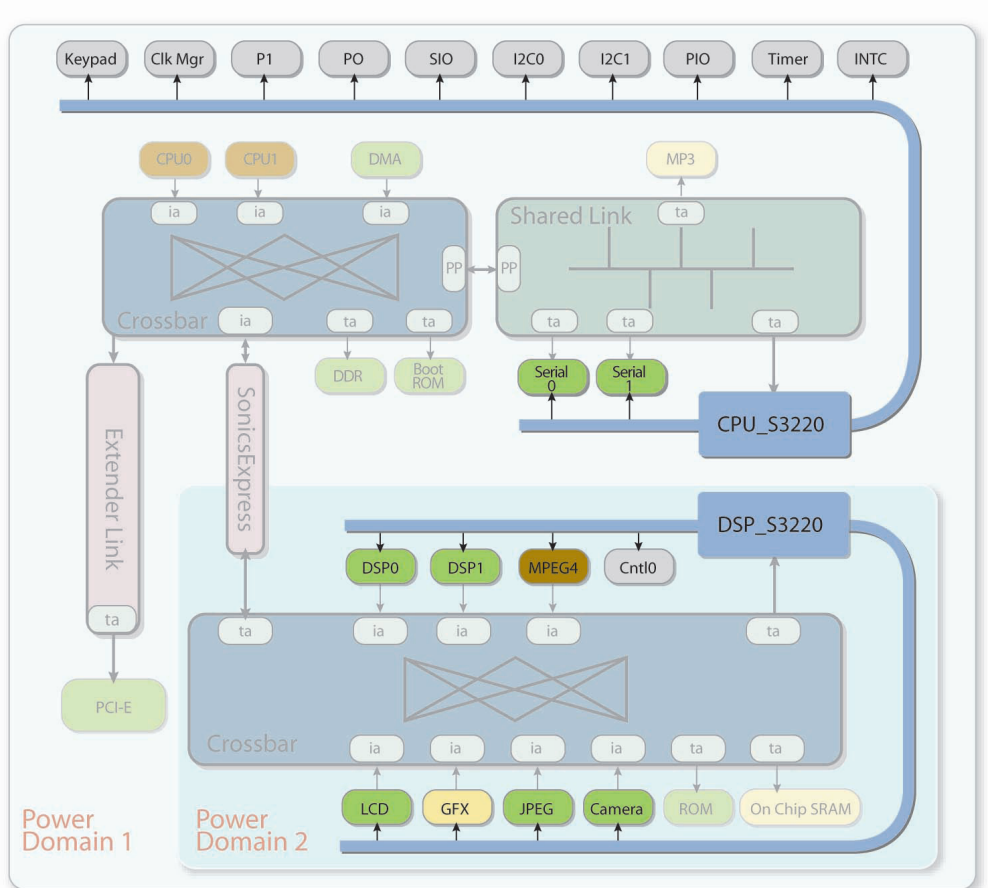
### Shorten Time to Market

- Preverified configurable solution already proven to interoperate with other high speed interconnect solutions
- Rapid integration of many IP cores spread across a die
- Pre-characterized interconnect eliminates timing closure uncertainties
- Reuse of cores through easy configuration with a high degree of automation

### Lower Power Consumption

- Low power physical structure
- Fine granularity power management

Sonics3220 SMART Interconnect solution is a non-blocking peripheral interconnect that guarantees end-to-end performance by managing data, control and test flows between all connected cores.



Providing low latency access to a large number of low bandwidth, physically dispersed target cores, Sonics3220 uses a very low die area interconnect structure that facilitates a rapid path to simulation.

This SMART Interconnect solution handles incoming traffic from up to four initiators and can distribute those communication requests and responses to up to 63 targets. By eliminating blocking, Sonics3220 allows multiple transfers to be in flight at the same time while producing a more predictable performance model for cores on a Sonics3220 system. Core service requests can occur whether there is an ongoing transfer or not. In addition, because the Sonics3220 is non-blocking, there is no need for a multi-layered bus architecture, thus reducing costs and power consumption.

Sonics3220 supports the industry standard Open Core Protocol (OCP) and AMBA Peripheral Bus (APB) interfaces.

## Features

To help create SoCs, Sonics3220 is packaged with SonicsStudio consisting of the SoCCreator GUI, interconnect support tools, and an adaptive testbench for validation. To surpass the limitations of current peripheral bus-based solutions Sonics3220 provides the following key features:

- A non-blocking interconnect with fair arbitration.
- Native support for OCP 1 and 2 sockets and support for AMBA interfaces available from Sonics.
- Design-time parameters that permit:
  - Up to four OCP-compliant initiators with a total of four OCP threads and up to 63 OCP-compliant targets.
  - Configurable address widths up to 24 bits.
  - Configurable data widths of 16 or 32 bits at the initiator subsystem.
  - Configurable data widths of 8, 16, or 32 bits per-target.
  - A choice of static endianness - big or little for the initiator subsystem including the Sonics3220 configuration registers and target agents with OCP2 sockets.
  - Fair arbitration with one optional high priority initiator thread.
  - Fully synchronous, divided, or asynchronous clocking for the target socket OCP interfaces.
  - Peak bandwidth of 332 MBytes/second at 166 MHz.
  - Best case latency of 1 cycle on request and 1 on response at 100 MHz.
- External hardware power management interfaces.
- Implements fine and coarse grained clock gating for low idle and active power.
- User configurable signaling between cores using OCP sideband signals.
- Resource locking support through OCP ReadEx/Write transactions.
- Optional error detection and recovery including:
  - Watch dog timers to identify unresponsive target cores.
  - OCP reset control for individual target core sockets permitting recovery using firmware.
  - Extended error logging to identify security access failures at initiators.
- Configurable access control for user defined address map regions based on initiator connection IDs and optional use of initiator request role information.
- Debug support (capturing transactions at a 1:1 clock ratio).
- Access security hardware that protects designated cores from access by unauthorized initiators, protecting media content and intellectual property.

