

Product Brief

Simplifies and improves AMBA based designs

- Provides a turn-key solution for SoCs that are dominated by AHB and APB cores; simplifying multi layer designs thus reducing customer design time and resources

Multi-protocol

- Supports AHB, APB along with upgraded sockets for AXI and OCP based cores

Low Latency

- Guaranteed bandwidth for latency sensitive peripherals
- 0-latency through the matrix
- Latency sensitive masters can be given priority for arbitration

Quality of Service

- Set data priority level through the matrix
- User controllable dynamic QoS

Design Capture

- GUI provides a simple, intuitive design capture interface
- Automation of RTL and synthesis script generation
- Automation of performance-testbench for bandwidth, latency, and power measurements

Low Power

- Improved master layer design to eliminate broadcast communications along with coarse and fine grain clock gating for the interconnect matrix

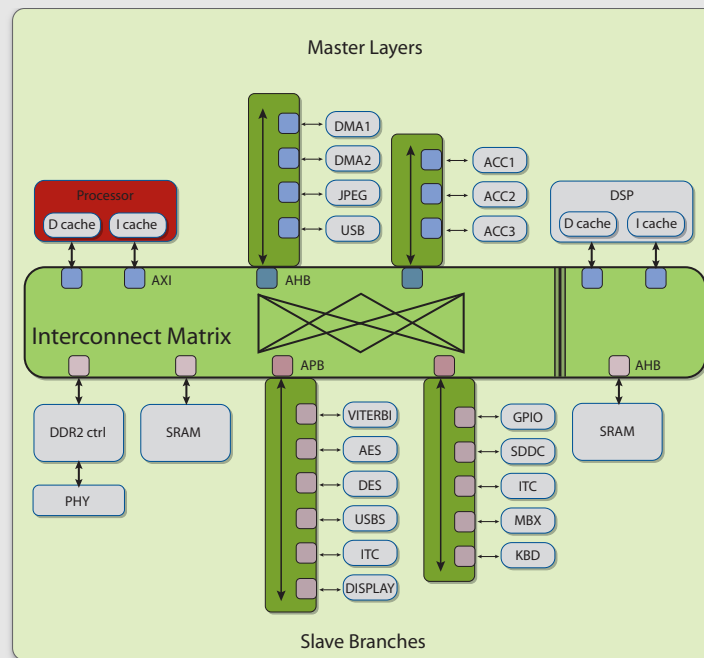
Efficient Power Management

- Automatic clock gating at fine and coarse grained levels.
- Split/merge architecture of matrix eliminates broadcast communications that are power hungry in ML-AHB
- Internal SRMD burst protocol saves switching power

Sonics' Network for AMBA Protocol (SNAP), offers SoC developers a low-cost, easy-to-configure bus solution specifically designed to simplify AMBA-based designs. SNAP's unique architecture makes it an attractive alternative for complex SoCs that are outgrowing traditional multilayer AHB designs. Users looking to improve AHB bus performance, facing memory bottlenecks or needing to integrate AXI with AHB/APB, or looking for better bus design tools and design methodologies will find SNAP an ideal solution.

The SNAP architecture consists of AXI and AHB master layers, AHB/APB slave branches and an interconnect matrix. Each element allows designers the flexibility to create the optimal system architecture by allowing the SoC to be configured for the best performance while minimizing chip area. SNAP tools provide an automated design environment to support architecture exploration so that performance, power and area trade-offs can be made.

The combination of SNAP architecture and tools provide a complete platform design that will shorten design cycles and save cost by allowing a high level of reuse. SNAP will grow with your design if there is a need for higher performance processors and memory.



The AXI/AHB master layers and AHB/APB slave branches provide better performance with efficient power consumption than traditional architectures. The master layers can support up to 8 AXI or 8 AHB masters per layer, while the slave branches support up to 16 AHB/APB slaves per branch. Performance improvements are made with custom arbitration in the AHB master layers allowing concurrent bus access for each core.

In addition to the master layers, SNAP includes a low-latency crossbar that simplifies multilayer AHB designs. High performance cores and memory can be connected directly to the interconnect matrix allowing the lowest latency and best performance. The interconnect matrix supports a wide range of popular interfaces, negating the need for extra bridges or additional validation. All protocol, data widths, and clock conversions are handled automatically. Optional pipeline registers support chip frequencies upwards of 266MHz (in 90nm libraries).

SNAP - Sonics Network for AMBA Protocol

SNAP's interconnect matrix permits direct blending of AXI and AHB masters and APB and AHB slaves without the large latency penalties often associated with bridging. It naturally supports simultaneous accesses to different targets and multiple outstanding requests to those targets. This is useful in optimizing peak bandwidths at important shared slaves. The matrix also allows each target to specify its own priorities for layer access.

Using an intuitive design capture tool, SNAP allows users to rapidly capture and analyze their SoC designs. The SNAP tools flow includes programs that run on both the client's machine and on Sonics servers. The advantage of this flow is that the user only need to download a small program called the SNAP capture tool thereby eliminating the need to deal with complicated license servers and license key files. All the RTL and test benches are generated by Sonics, greatly reducing the installation burden.

The capture tool provides a graphical user interface along with tabular data input. This tool has two functions: help the user capture the configuration of the SNAP instance to be generated, and create a set of files that describe this configuration. The output of the SNAP capture tool is the list of captured values that is then sent to the SNAP server at Sonics for RTL generation and other processing.

The interconnect configuration is captured using a block diagram entry for the topology, and a set of tables for internal parameters. The block diagram allows the specification of initiator and target cores along with the type of interface required (AHB, APB, AXI, etc.). To further simplify the design effort, the tool will pre-compute most of the design parameters based on the user optimization requirements. These optimizations include options for gate count or performance.

