

## Product Brief

### Reduces SoC Cost

- Optimized interconnect provides advanced features with low gate count
- Small generated logic clusters ease maximum SoC core packing

### Simplifies SoC Design

- Multi-threaded and non-blocking communications
- Seamless connection to OCP, AHB, and AXI based cores
- Full user control of latency, performance, and area
- Advanced power management support including clock gating

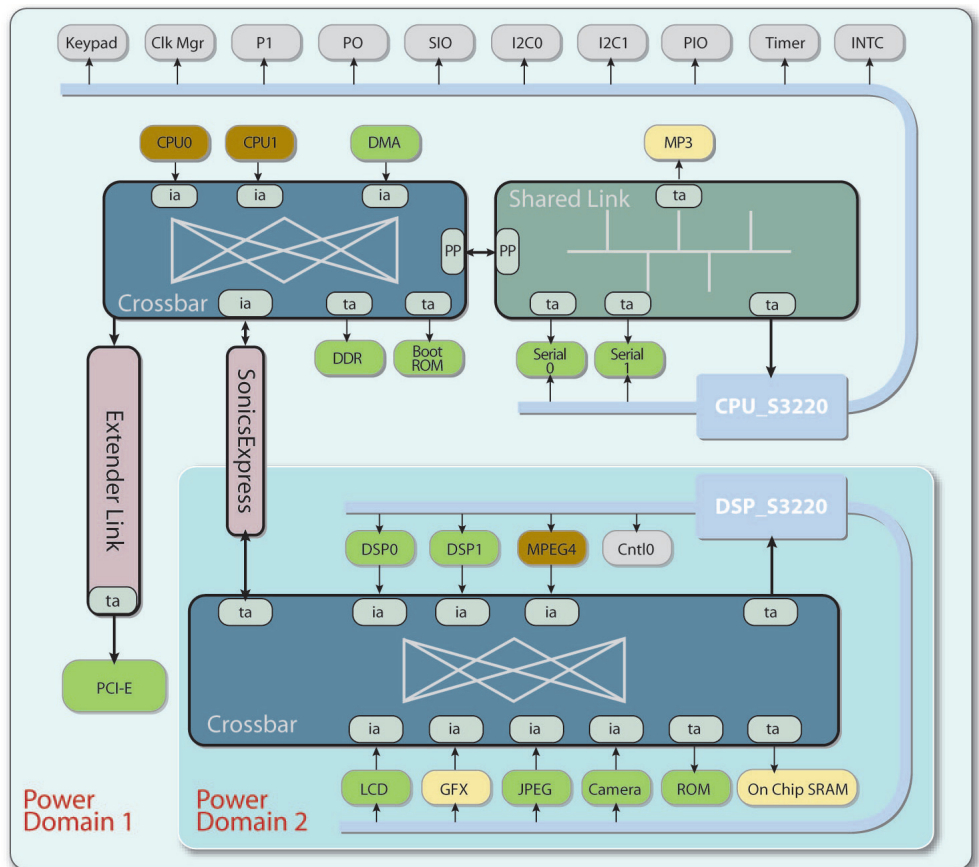
### Accelerates Chip Time to Market

- Socket based design enables parallel design of SoC cores and interconnect while guaranteeing high SoC core reuse for future product derivatives
- SonicsStudio development environment automates interconnect configuration, data analysis, and performance verification for faster architectural design cycles
- SonicsMX SystemC model unifies system and RTL outputs from one design

### Accelerates Product Family Development

- Simplified SoC core reuse
- Flexible subsystem-based partitioning

The SonicsMX SMART Interconnect solution contains a high performance advanced fabric and a comprehensive set of data flow services for the development of multicore SoCs. By utilizing state-of-the-art physical structure design and advanced protocol management, SonicsMX delivers guaranteed high bandwidth together with leading edge, fine-grained power management. Quality of Service, access security, and error handling features comprise a robust turn-key solution that facilitates higher design predictability and decreases chip development time.



■ AHB ■ AXI ■ OCP

Supporting multi-threaded and non-blocking communications, SonicsMX offers both crossbar and shared bus structures in an innovative distributed implementation. Compliance with Open Core Protocol (OCP), AHB, and AXI interfaces ensures maximum reuse of all cores regardless of their native configuration.

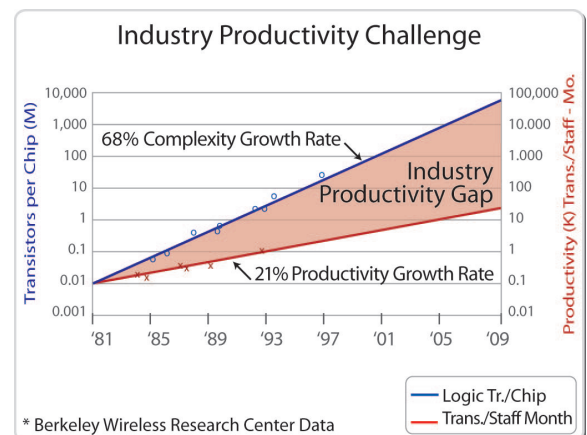
SonicsMX decouples the functionality of each core from the interconnect communications required among the cores. Configuring SonicsMX allows SoC developers to tailor the communications for each core's specific needs while balancing latency, physical layout, clock frequency, area, and power consumption.

The SonicsStudio<sup>™</sup> development environment supports SonicsMX by automating configuration, data analysis, and performance verification. A SystemC model is available to allow architectural modeling concurrently with application software development.

## Features

SonicsMX is a member of the Sonics family of SMART Interconnects. Complimentary products include MemMax®, a DRAM scheduler that minimizes latency to DRAM and optimizes throughput, and Sonics3220™, an I/O interconnect that off-loads slow transfers from the system interconnect. These products create a complete turnkey solution for all SoC data flows.

- A total of 64 sockets can exist on each SonicsMX instance.
- Configurable to provide a full (or partial) cross-bar or a shared link topology.
- A highly flexible structure to accommodate latency sensitive portions of the system.
- User-specified connection map, address map, and command map.
- Permits internally shared paths.
- Natively supports OCP 2.x sockets, and provides interfaces to OCP 1.0 sockets, AXI 3.0, and AMBA AHB-lite 2.0 sockets.
- Implements dynamic endianness aware width conversions.
- Configurable address widths up to 64 bits.
- Target decoding down to a granularity of 1 KB.
- Configurable protected regions within address space.
- Configurable data path widths (sockets and internal) 16, 32, 64, or 128 bits. Four to one range of widths allowed within any instance.
- Peak bandwidth limited only by target limitations.
- Accommodates synchronous and synchronous-divide clock rates for each socket.
- Permits clock rates of up to 300 Mhz subject to configuration choices in 90nm libraries.
- Flexible internal pipelining makes frequency independent of span.
- Supports 0 cycle minimum latency paths.
- Supports sideband signaling for interrupts, errors, and power controls.
- Scalable frequency, trading off interconnect span against latency by adjusting the depth of the interconnect pipelines.
- Power management interface coordinates voltage or clock removal.
- Implements fine and coarse grained clock gating for low idle and active power.
- Monitors for software error conditions (unsupported commands, protection violations, addressing errors) and protection violations.
- Monitors for failing cores (timeouts).
- Performs error logging and recovery support.
- Optional debug ports to probe operation of internal paths.
- Dynamically configured access protection (firewall) for cores or memory regions against access by specific initiating cores or processes.
- Separate request and response networks that adapt easily to targets with long or unpredictable latency (such as DRAM systems).



SonicsMX has provided a 15X productivity Improvement in customer deployments.