White Paper

New Interconnect Definitions that Address the Impact of Convergence on SoC Design Methodology

Introduction

The mixing of communications and multimedia processing onto a single chip ("convergence") has substantially increased design complexity, which is rapidly rendering traditional SoC development methodologies obsolete. The escalating time and cost to engineer and validate a design is proving this out in many cases today. One of the major causes is the rising complexities associated with the SoC interconnect architecture, and the need to re-tool this area of design to remain competitive.

This white paper explores the issues and choices in re-tooling SoC development methodologies. The conclusion is that a shift to Data Flow Centric "Platform" SoC development with the centerpiece being an outsourced Interconnect architecture best accommodates the multi-core processing requirements necessary to support today's system features within shrinking timeframes to remain competitive. No longer can SoCs be designed by starting with a processing element and building the rest of the chip as an approach. In order to determine what system features can be accommodated in the design, the Interconnect architecture must first be in place to enable the complex mixing and matching of the processing elements that supports the overall system design and validation.

A shift to Platform SoC design reorients the design tasks in such a way to minimize validation and risks. This white paper shows how this shift has a direct positive impact on time to market and development costs. The first section addresses how the semiconductor industry has changed and what are the new keys to success. The second section will offer some questions and answers designed to help SoC developers determine what changes are necessary in SoC development methodology to remain competitive.

Section One A Changing Industry

The Semiconductor Industry is in the midst of a major transformation, impacting every aspect of the business. For SoC developers, digital consumer and wireless communications markets are booming, and geographical shifts in volume consumption are causing companies to focus on world wide market strategies. Since these new industry dynamics are radical departures from the old dynamics, they are also causing many of the fundamental processes and structures associated with semiconductor development to change. Making money has a very different formula today than it did in the past.

Convergence Finally Arrives

HDTV, Mobile TV, IP Set Top Boxes, and Mobile Entertainment PCs are now lucrative products in key growth markets. What does this mean? The long awaited convergence of digital media streaming and communications has finally arrived, and represents the best opportunities to make money looking ahead. Every aspect of the industry is reacting to this convergence in some way. The key question for SoC developers is how does this impact the transformation of the requirements to be expressed in silicon?

Integrate or Die

What used to be several chips on a board is now one or a few SoCs. The accelerating price pressures on the systems business today make consolidation of system functions a must. Early entry into new market segments is paramount to success (the ability to beat competitors to market, capture premium sockets and achieve acceptable return on SoC development investments). These are today's SoC project drivers.

However, a new phenomenon has emerged that makes these new trends so much more difficult to manage. With downward price pressure, fewer sockets per system (a by-product of convergence), and shortening life cycles, there is escalating complexity. Therefore, even though "premium" market windows are shortening and price erosion accelerates, design complexity is exploding. The new mantra then is "integrate or die".

In order to compete then in today's SoC world, several things must change:

1. SoC developers must integrate digital video, audio, and data onto a single chip faster than the competition.
2. SoC development projects must be architected such that their costs can be amortized over many chips, in order to accommodate increasing price pressure and to address time to market, all while remaining profitable.
3. Fundamental SoC design methodology must accommodate the massive increase in design complexity under the new market dynamics (how to

integrate multimedia streaming and communications, and how to achieve enough bandwidth from off chip memory to make it all work as a system)

Platform SoC Development Now A Requirement

Many of the semiconductor leaders in their markets have already re-engineered their fundamental SoC development methodology. Companies such as Broadcom (leading provider of 802.XX devices), Texas Instruments (leading provider of OMAP application processor chips to the cell phone market), Toshiba (leading supplier of digital consumer devices for gaming and home entertainment), and Samsung (leading provider of digital television and cellular phone solutions) are examples. The key element in all cases was their fundamental shift to a Platform SoC methodology.

What Does Platform Centric SoC Methodology Mean?

Processor centric SoC design has been the mainstay SoC development methodology pre-convergence. Simply put, it means choosing the processor as the critical element of the SoC development project, and supplementing with processor bus architectures and much less complex logic blocks to complete the device.

Interconnect SoC architecture is the basis for Platform SoC methodology. Here, the Interconnect architecture becomes the most critical choice for the SoC development project. Complex logic, such as microprocessors, digital signal processors, and multimedia engines, all connect and interact through the Interconnect. External memory access is also managed through the Interconnect.

The Impact on Changing SoC Development Methodologies

When the most important decision for the dominant number of SoC development projects world wide consisted of choosing a microprocessor designs were difficult but manageable. Reusing any of the blocks was a bonus, but redesigning the chip for each derivative while also difficult was still manageable. To provide some assistance, tools emerged to help the EDA flows by automating some of these simple tasks. However, the introduction of convergence into today's SoCs has brought about several new complexities not present before and are not addressed by bus generators, leaving a much higher burden on the SoC developer to complete the tasks:

1. The emergence of multiple complex logic blocks, each with different processing needs (microprocessor latency dependencies vs. media engine bandwidth dependencies for example). SoC Interconnects now

require support for multiple interfaces, complex arbitration schemes, and quality of service management to keep all aspects of the system running properly.

2. Multiple blocks also demand access to external memory and with different requirements. More advanced arbitration and scheduling is now required to minimize memory access starvation and maintain high processing element utilization. Given the high total cost (performance, power, area) of these processing elements, high utilization is a must.
3. Since these complex blocks have different needs, there is an added complexity to the SoC design that must address error and interrupt management, how their power consumption is managed, and how security aspects are managed. How are all these controlled?

These facts establish that the shift in risk and cost in any SoC design project now lies in the complexities brought about by convergence. The choice of processing elements, while important are more manageable engineering tasks in comparison with the work necessary to put the blocks together and make the multiple flows work as a system.

What has emerged as a result is the need to retool the development methodology to an Interconnect centric approach. The most critical decision for this re-tooling then is whether the in-house development team assumes the burden and risks of developing the complex SoC Interconnect, or can this activity be outsourced and purchased as configurable intellectual property to lower the burden on the design team and to lower risks. While this decision has technical ramifications the real question given market delivery pressures is what makes business sense?

In-house developed interconnects can only be verified near or at the top level of the SoC design, late in the development cycle. Since the complexity of the interconnect design is much higher today, the risk of a late discovered bug is also much higher, and the recovery time can be much longer. In house development therefore builds in high risk to the project. One spin could cost months, which may be the difference between a highly profitable project and one that loses money. Outsourcing reduces risk because the required features are pre-verified and tools are available that enable that interconnect design and validation to occur during architecture exploration, long before logic and physical design. This shift significantly reduces the risks.

Sonics Innovative Approach to SoC Development

Sonics is the premier supplier in the Interconnect segment of the Semiconductor Intellectual Property (SIP) market. Sonics offers SMART Interconnects and Memory Management products that facilitate the rapid development of Systems on A Chip (SoC) for embedded systems markets. SMART Interconnects combine advanced fabrics and complex data flow services that replace the need for SoC developers to design, verify and maintain similar complex functions on their own. These features are seamlessly integrated into a flow that allows for adjustments of the parameters required to resolve the design problems.

SMART Interconnects allow SoC developers to shift interconnect and IP validation to the architectural phase of the chip development process, enabling a clear understanding of the data flow issues early in the project. When coupled with a memory management product from Sonics, SoC developers also enjoy rapid resolution of key system issues, such as latency and bandwidth optimization to and from external memory, which further streamlines the development process and lowers risks.

The utilization of Sonics' products has demonstrated repeatedly that SoCs can now be developed in a fraction of the time and at a fraction of the cost when compared to architecting interconnect solutions in house.

Advanced Fabrics

Advanced fabrics upgrade traditional bus fabrics to meet today's SoC requirements. There are several distinct features of advanced fabrics that distinguish them from interconnects that are a product of bus generators or the typical in-house solution.

1. Advanced fabrics are non-blocking. Traditional fabrics were originally architected with the Processor centric SoC model in mind. Today the introduction of Data Flow centric "Platform" SoCs, which contain many complex cores and even several hetergeous processing elements, introduces the requirement of balancing bandwidth and latency across more than one processing element. Traditional bus fabrics block one or more of these elements from processing data. This introduces performance interdependencies that complicate design and analysis of the system, and add to development costs, time to market, and risk. The resulting SoC is filled with compromises to meet time to market.

   The non-blocking nature of advanced fabrics minimizes performance interdependencies by implementing more effective communications schemes within the Interconnect. Superior performance is achieved without incurring area and power penalties when compared to traditional fabrics plus the additional logic necessary to achieve similar results.

2 Advanced fabrics decouple cores from one another. Traditional fabrics tightly couple the communications schemes of each of the cores connected to the fabric. This was okay when the number of cores on the chip was low. However, the explosion of core counts forces SoC developers to re-engineer major portions of the SoC for each derivative in

the product line. This creates enormous re-engineering costs. Advanced fabrics decouple the cores, enabling SoC developers to isolate re-engineering to only the functions that are changing within each derivative product, facilitating efficient Platform SoC development.

3 Advanced fabrics support universal core connectivity. Traditional bus fabrics require all cores to conform to one protocol for connection to the bus fabric. But with many choices in the market, such as ARM AMBA, OCP, and in some cases the need to maintain internal protocols for key competitive advantage, SoC developers are often faced with the need for multiple protocol support. Protocol bridges are traditionally developed to support the various core connections. However, these bridges introduce yet more cost and risk to the design. Advanced fabrics eliminate the need for bridges by employing socket based connection points that can be configured for virtually any protocol. This enables the mix and matching that is required of today's SoCs given multiple sources for all the IP cores.

4 Advanced fabrics offer upward compatibility with Interconnects that also offer data flow services. In most cases today, Platform SoC projects span a wide range of functionality. High reuse must be maintained. A product family may start with only the need for an advanced fabric that evolves into the need for data flow services to support higher complexities. Advanced fabrics separate the needs of the fabric and the data flow services in such a way that a range of complex SoCs can be developed while maintaining maximum compatibility, regardless of the data flow services required

5 Advanced fabrics facilitate the Interconnect development as part of the architecture exploration phase of the SoC development cycle. Traditional bus fabrics today are verified as part of the final tasks of the SoC cycle. Because their complexity has risen dramatically, validating their functionality and performance at this late stage of the cycle has become high risk. Re-engineering can take months. Advanced fabrics are accompanied by tools that support shifting the development and verification of the Interconnect to the architecture phase of the cycle. This significantly reduces verification times and enables SoC developers to predict Interconnect behavior before the physical design cycle begins.

Data Flow Services

Those SoCs which contain multiple heterogeneous processors (MPUs. DSPs, multimedia engines) often require more management of the data flow than traditional bus fabrics or even advanced fabrics offer. The lack of data flow services in many products today leaves their development to the engineering team This means any adjustments to the solution can cause projects costs to explode and introduces high schedule risk, as these services are non-trivial and frequently debugged during the final chip integration. Sonics SMART Interconnects are the only commercially available products today that offer both advanced fabrics and data flow services.

What are data flow services?

1. Quality of Service. Perhaps the most important aspect to distributed heterogeneous processing architectures today is how to get all the tasks on all the processors to meet the system requirements, especially when they are all combined onto one chip. Emphasis on complex QoS methods forces development teams to spend a significant amount of time and energy to architect a solution. The solution obtained is often optimized for the specific problem being solved at that time due to schedule, resource, and tools constraints. This must be re-engineered with each derivative. The introduction of QoS as a data flow service by Sonics enables SoC developers to exactly fit their functionality and performance schemes “like a puzzle” while lifting the burden of support and scaling from the development project.
2. Power Management – Often viewed as both an art form and a science, every chip development project today has some need for power management. By accessing the advanced schemes employed by Sonics, SoC developers often achieve far better power management results.
3. Error and Interrupt Management. Today, each of the processing element types (uP, DSP, and multimedia engines) has different computing structures. This introduces a wide variety of exception handling which can consume lots of development time to resolve. This is necessary for robustness, but buys nothing in performance. Having an interconnect that pre-organizes all the error cases, and raises the level of abstraction for managing them saves considerably in design time/cost The availability of a data flow service that can “snap in” to the schema for each of the processing elements, and be different for each of the elements connected to the interconnect, ensures proper management of the entire system when in real time.
4. Data width conversion – Another key element to heterogeneous processing architecture is the fact that each of the processing elements gives and takes data in their own way, optimized for their own processing environment. Data width and endianess conversion data flow services further the “snap in” method of interconnect to core connection by also managing conversion of the data, transparent to each of the cores and on the fly, while minimizing the performance impact on the entire system.
5. Firewalls and advanced security management – Mixing communications and multimedia content on the same chip often leads to a wide variety of security needs. Similar to PC based networks, these “network on a chip” interconnects must provide adequate protection of the content they

process. It starts with configurable firewalls, but today often includes digital rights management, the fundamentals of which must be managed by the very “channels” that move the data. The introduction of security management data flow services ensures that SoC developers can meet aggressive system requirements, which often change from system vendor to system vendor, without re-engineering implementation schemes.

6. Side band signaling management – When considering the control of multiple processors and an array of cores on a given chip, typical architectures today can result in significant “overhead” which is paid in area and performance, due to controlling functions. While playing an important role in the operation of the chip, these functions rarely contribute directly to the operation of the functions at the end user level. By utilizing side band signaling, this overhead can be minimized, which saves in performance and area, and pay big dividends on final chip size.

Integration and Validation: Another Rising Dimension of Risk

Another important aspect to complex SoC development is the growing risks associated with integrating all the IP (bought or made) and the huge costs associated with top level validation. Traditional SoC methodologies use an IP building block approach. Since these blocks are typically sourced from multiple vendors (or even multiple departments within a company), they are not all designed the same. The SoC integration effort must therefore accommodate the differences in order to validate the collection of the blocks. Somewhat irrespective of the interconnect make versus buy decision promoted in this white paper, integration and validation tasks are expensive and come with very high risk.

Sonics has developed a risk management approach for integration and validation. Sonics provides a comprehensive tool, called SonicsStudio, which enables SoC developers to configure and test Sonics Interconnects. While providing a convenient way to use Sonics products, the true value of the tool is that it shifts all the risk of the Interconnect design to the architecture phase of the design cycle. The ability to verify the operation of the Interconnect specifically configured for the given design dramatically reduces the risk of failure during the verification phase of the physical design. Mitigating these risks therefore is achieved with use of the tool.

Since design and verification is now part of the architecture phase of the cycle, the tool can also be used to model many derivatives of the “base” design before any of the devices are produced. This supports the Platform SoC methodology by giving designers critical insight into product line development.

Changing the Way Business is Conducted

The transition to a Platform SoC strategy is a must today to compete. The two key elements in this transition is to lower design risks and reduce development costs. Given exploding complexity, the new phenomenon identified signals that new approaches must be taken.

The first decision in the transition is the SoC interconnect architecture. This section of the white paper has discussed the issues and concluded that outsourcing the architecture makes the most business sense. It is worth noting that it is somewhat irrelevant that technically equivalent solutions could be designed and maintained in house, the risks and cost burden associated with the make decision are no longer economical given the potential downside.

The second decision is in the ability to reduce top level integration and validation risks. It is necessary to shift the interconnect design to the architecture phase of the development cycle in order to lower these risks. A by product of the shift to a Platform SoC methodology is the ability to add more intelligence to the IP core choices based on a working detailed data flow models.

Sonics SMART interconnects solutions directly addresses both decision points by offering advanced fabrics and data flow services that are designed for today’s SoC requirements. SonicsStudio enables the integration and validation shift to the architecture phase of the development cycle.

Imagine being able to react to a key market need in weeks at a fraction of the development cost when compared to spinning a chip using traditional methodologies. The impact on sales and marketing are far reaching. This is the ultimate benefit of the transition to Platform SoC development using Sonics as the interconnect provider. This is why leading semiconductor company’s using Sonics today are winning in their markets.

Section Two: Assessing the SoC Development Process

This section is offered as a template for assessing whether the SoC projects being undertaken are exposed to some of the design problems associated with convergence and to help determine whether it is more economical to outsource the interconnect design.

The following series of questions are offered as a guide to the assessment. These questions represent some of the top level issues that SoC developers will encounter:

1. Can all critical IP cores access the interconnect at all times?

Performance requirements are high and in many cases the processing blocks chosen are expensive in power and area. Given increasing price pressures, it is imperative that the chosen processing elements reach as close to maximum utilization as possible. This ensures system level performance remains adequate and also relieves the "tight code" burden often placed on software development.

Traditional bus architectures were designed essentially for only one complex logic block. Adding more than one often times creates blocking. Today's SoCs cannot afford starvation (imagine a media processor not getting access to its next MPEG block for processing when it needs it). Buffering schemes and system effects to accommodate blocking architectures, given the complexities of convergence, introduce tremendous development time, cost and risk. It is not necessary anymore given that Interconnect based SoC architectures are available that are non-blocking.

2. Can IP cores be decoupled from one another?

High reuse of all logic blocks, simple to complex, is now a requirement so that re-engineering costs for derivative designs are minimized. In traditional bus architectures, where the function of the block and its communications to the other blocks (given the bus is just wires) is tightly coupled, any change to a block constitutes a whole new design process.

By decoupling the communications of the cores, the task of communications can be shifted into the interconnect and controlled uniformly. Now isolated blocks, including the interconnect, can change with little or no effect on all other blocks. Reuse is maximized.

3. Does the Interconnect provide universal core connectivity?

Any strategy that includes acquiring a complex block from outside will inevitably be designed NOT to fit into the traditional interconnect. Traditional bus architectures force SoC developers to maintain bridges between the block and the Interconnect, and the management of the bridge from a system perspective. With complexity exploding the opportunity for many such bridges poses a high ancillary design cost and risk (functionality and performance) on the developers.

Sonics supports universal connectivity. That is any AHB, AXI, or OCP based block can be seamlessly connected to a Sonics Interconnect. This eliminates the costly bridges and side work required to manage the system design.

4. Is the interconnect upgradeable?

Does anyone really know exactly what they are going to need to build next generation? The digital consumer and wireless communications trends, with fragmenting market segments and changing standards suggest that flexibility is a key factor for new design methodologies. Since the interconnect is centric to the methodology, this is first priority.

Traditional interconnects are not upgradeable as they relate specifically to the layout and timing of one specific device. In contrast, Sonics offers several products based on a common technology designed to ensure that upgrading is straight forward. This gives SoC developers the ability to design a vast array of devices while preserving investments every step of the way. Compatibility also enables swift decisions with manageable risks as market conditions change. By upgrading the interconnect and changing a few blocks, new businesses can be entered rapidly with minimal re-engineering.

5. Are tools available that enable Interconnect design to shift to the architectural phase of the SoC development cycle?

Section One discussed the need to shift Interconnect design to the architecture phase of the SoC development cycle to reduce verification and closure risks. Additionally, the ability to "what if" the Interconnects during architecture exploration greatly improves the flexibility of the entire methodology. This is highly advantageous for derivative development given the rapidly changing market requirements brought about by convergence. This aspect of the new methodology may well have the largest impact on success; because it greatly softens the need to have exact specifications well before chip design and certainly enable straight forward changes as the product line development strategy unfolds.

Getting the Most out of Changing the SoC Development Methodology

When comparing these questions against a SoC development methodology path, if the answer to any one of these questions is NO, then the path is not the most efficient and effective compared to a Platform SoC approach based on Sonics SMART Interconnects. With each additional NO answer, the risks and burden on the SoC development team increases exponentially because of the interdependencies associated with managing the system level effects of each NO.

In the end, the development process should be the best it could be. This means a methodology with all YES answers is the most logical choice. Only Sonics can provide all YES answers today.