

Product Brief

Increases SoC Performance Up to 400 MHz @ 130nm

- Guarantees Quality of Service (QoS) for on-chip cores
- SRMD & MRMD support
- Supports up to eight banks in one DRAM, adds bank busy flags to memory interface

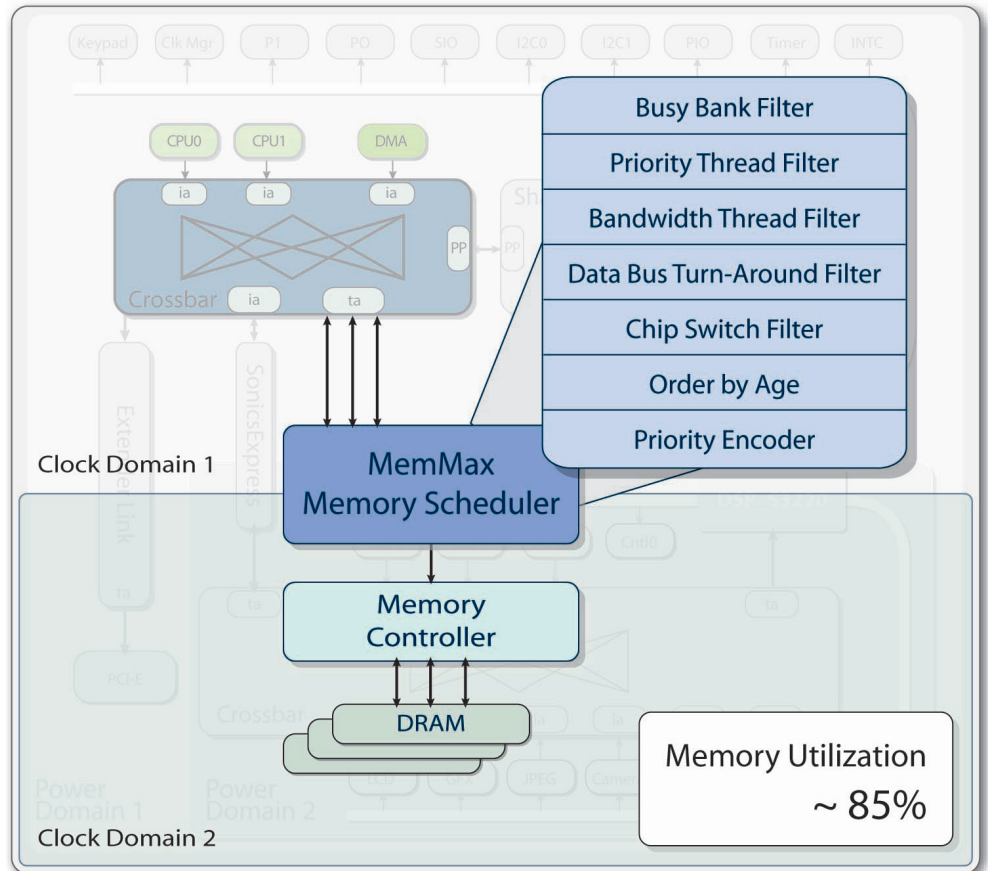
Lowers SoC Costs

- Consolidates and reduces multiple distributed buffers

Shortens Time to Market

- DRAM technology selection decoupled from the rest of the SoC
- Multi-threaded architecture enables easy scalability without redesign of memory subsystem

The MemMax Memory Scheduler is an intelligent DRAM access scheduler designed for use with an OCP compliant memory controller and Sonics SMART Interconnect™ solutions.



Ideal for high-bandwidth applications, MemMax's sophisticated thread-based pipelining and advanced arbitration schemes reduces interconnect over-design and redundancy. By decoupling the functionality of the SoC from the DRAM, MemMax also encourages adoption of the DRAM technology that offers the best cost and performance value.

SoC designers can use compiled RAM to consolidate all of the flip-flop based buffers normally distributed among the various initiator cores into a single buffer within MemMax. This reduces the total SoC die area and lowers overall power consumption. When used with a Sonics SMART Interconnect solution, MemMax further reduces SoC costs by eliminating a substantial amount of the excess wires required by traditional wire-based, multi-layered bus architectures.

Features

The Sonics MemMax Memory Scheduler improves overall SoC performance and reduces costs by intelligently managing access of off-chip DRAM. Features include:

Improved DRAM efficiency

- Thread-based scheduling maximizes overall DRAM efficiency and provides levels of quality of service for the different threads. With no ordering requirements between threads, requests from different threads can be freely re-ordered.
- MemMax reduces timing costs from DRAM data bus turn-around by grouping similar accesses, (i.e., writes with writes and reads with reads).
- Scheduling accesses to on or off-chip DRAM mitigates inefficient switching between banks of physical DRAM.
- Configurable filtering algorithms sort conflicting scheduling goals. Each filter looks at valid requests from all of the threads and filters out requests based on the filter's function.
- Essentially memory independent, MemMax can work well with a DDR controller, DDR-2 controller or even a XDR controller.
- The scheduler is designed to work in bank-interleave mode and page-open mode. The underlying controller can offload all the scheduling logic to MemMax.
- Clock gating can be used to lower power consumption by several orders of magnitude.

Quality of Service (QoS) modes

- System data flows are supported with different service qualities (best effort, allocated bandwidth, and priority).

Scheduling

- MemMax arranges requests to avoid events that interfere with a smooth, pipelined flow of operations in the DRAM. The scheduler issues requests to the controller in a short, configurable DRAM block size that is

typically set to match the DRAM burst length. To increase efficiency, the scheduler employs the largest OCP burst size up to the configured DRAM block size.

Fully configurable

- The user can choose the sizes of the buffers, modes of operation, QoS settings that best suit his application.
- MemMax can trade-off high memory utilization, with low latency requirements. Each incoming thread can be assigned a runtime programmable QoS value. Based on this value, MemMax assigns a corresponding priority to the thread, ensuring low latency traffic.
- Scheduler features including memory and buffering can be configured. Registers in the DRAM controller may also be configured.

Interconnect compatibility

- By allowing fine-grained interleaving of requests from different initiators, the interconnect eliminates the need for high-bandwidth bursting and bandwidth-matching buffers in the initiators.
- Exact threadbus flow control is applied to all OCP phases (request, data, and response) to ensure non-blocking behavior.

Open Core Protocol

- Support at system and memory interfaces enables simple swapping of alternate DRAM technology controllers (e.g., SDRAM, DDR, etc.) without requiring redesign of MemMax or the supporting interconnect.

SystemC Models

- Fast assessment of design trade-offs.
- Allows concurrent application software development.