



# EE Times

ELECTRONICALLY REPRINTED FROM JANUARY 4, 2010

## Viewpoint: Need to move beyond the network-on-chip

By Ray Brinks

Over the last decade, designers have been content with standard connectivity methodologies to fulfill the needs of their system-on-chip (SoC) designs.

With today's design starts using 65nm design rules or smaller, the number of cores in an SoC can exceed 100. Connecting 50 or 100 cores breeds challenges that SoC design teams did not have to previously face.

The inherent communications between on-chip cores is now taking on more of the comprehensive characteristics of a network rather than simply a bus. These characteristics include standard interface protocols, sockets at the edge of the network to allow cores to maintain a level of independence, and scalability so that the network can grow or shrink as needed. Enter the network-on-chip (NoC).

NoC technology provides a serialized on-chip network using a packetized protocol through a series of routers.

But will the NoC alone be the Holy Grail for on-chip connectivity or is there something bigger and better beyond the NoC?

Although the analogy of a network-on-a-chip is useful when describing NoC technology, it eventually breaks down when looking deeper into data traffic patterns and real-time performance requirements.

To optimize routed network performance, there needs to

be network-level concurrency in the traffic flow.

When looking at the traffic flow in a typical SoC, however, it is heavily weighted toward the DRAM (typically greater than 50 percent) — not distributed evenly across the network.

Additionally, many cores in a real-time embedded system are extremely sensitive to long latency paths which can be introduced by a NoC.

Careful placement of each core has to be done to insure that long physical spans are not created, thus introducing further delay into the system along with physical design problems.

Moving beyond the NoC allows designers to blend the best of several advanced on-chip network technologies to give them the freedom and performance options necessary to build value-added SoCs — and keep pace with the rapidly moving consumer electronics market.

To move beyond the NoC, designers must have access to the mix of connectivity technologies to choose the optimum topology solution for a given set of cores. A 4G baseband chip with approximately 50 cores serves as a good example.

There are a handful of devices that need deterministic access to the DRAM (e.g. CPU and DSP). The connection between these cores would be optimized by a low-latency high-speed cross bar. Other cores like the video processor that have some tolerance for latency can be grouped together with routers. This will provide the fewest



wires and allow the system to scale as cores are added.

Finally, peripheral cores are better served by a serial network that is designed to span long distances on the chip, freeing designers from concerns of the physical layout.

Moving beyond the NoC ultimately translates into the most practical of goals: optimized design team productivity, time-to-market and the most effective trade-off of SoC performance and cost.

### **Ray Brinks, Vice President of Engineering**

Ray Brinks has served as Sonics' Vice President of Engineering since 2004. Previously, Mr. Brinks was Executive Vice President and General Manager of the SoC Division at MosChip Semiconductor. From 2002-2003, Mr. Brinks was President of Veracity Technologies, an IPsec security device company. Prior roles include ZF Micro Devices, where he served as CTO/Vice President of Engineering from 1997-2002. Additionally, Mr. Brinks was with International Business Machines Corporation for 15 years in roles of progressive responsibility, including OEM Engineering Manager. He received a B.S. in Electrical Engineering from the University of Michigan and an M.S. in Electrical Engineering from the University of Arizona.



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